SAFETY PRECAUTION

The following precautions should be observed when servicing:
1. Since many parts in the unit have special safety related characteristics, always use genuine Hitachi’s replacement parts. Especially critical parts in the power circuit block should not be replaced with other makes. Critical parts are marked with □ in the schematic diagram and circuit board diagram.
2. Before returning a repaired unit to the customer, the service technician must thoroughly test the unit to ascertain that it is completely safe to operate without danger of electrical shock.

KEY TO ILLUSTRATIONS

1. PLAYBACK INDICATOR
2. REC INDICATOR
3. PAUSE INDICATOR
4. REC MUTE INDICATOR
5. TAPE COUNTER (TAPE COUNTER)
6. DIGITAL PEAK LEVEL METER
7. PEAK HOLD SWITCH
8. RECORDING LEVEL CONTROLS (RECORD)
9. MIC JACKS (MIC)
10. OUTPUT LEVEL CONTROL (OUTPUT)
11. MONITOR SWITCH (MONITOR)
12. DOLBY NOISE REDUCTION SWITCH/MPX FILTER SWITCH (DOLBY NR)
13. AUTO-REWIND SWITCH
14. MEMORY SWITCH (MEMORY)
15. EJECT BUTTON (EJECT)
16. REC MUTE BUTTON (REC MUTE)
17. PAUSE BUTTON (PAUSE)
18. RECORD BUTTON (REC)
19. STOP BUTTON (STOP)
20. FAST-FORWARD BUTTON (▶)
21. PLAYBACK BUTTON (▶)
22. REWIND BUTTON (◀)
23. HEADPHONE JACK (PHONES)
24. TIMER SWITCH
25. POWER SWITCH
26. BATTERY INDICATOR (BATT)
27. TEST INDICATORS
28. TEST START BUTTON (TEST START)
29. TEST MEMORY BUTTON
30. TAPE SELECT MEMORY BUTTONS
31. TAPE SELECT BUTTONS

STEREO CASSETTE TAPE DECK

January 1980
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</table>
SPECIFICATIONS

Semi-conductors:
ICs: 20
Transistors: 71 (U, C)
72 (W, FS, BS, AU)
FETs: 2
Diodes: 85 (U, C)
87 (W, FS, BS, AU)
LEDs: 15
Varistors: 2 (U, C)
3 (W, FS, BS, AU)
Micro computer: 1

Track System:
4 track 2 channel stereo
Tape: Cassette tape (C-30, 60, 90)
Tape Speed: 4.75 cm/s

Recording System and
Bias Frequency: AC bias, 105 kHz
Erasing System: AC erase
Erase Ratio: 65 dB or more (at 1 kHz)
Frequency Response:
Manual:
UD-ER (NOR) 20 Hz - 20 kHz
30 Hz - 18 kHz (±3 dB)
20 Hz - 20 kHz
UD-EX (CrO₂) 20 Hz - 22 kHz
30 Hz - 19 kHz (±3 dB)
20 Hz - 20 kHz
FeCr 20 Hz - 20 kHz
30 Hz - 18 kHz (±3 dB)
20 Hz - 18 kHz
Metal: 20 Hz - 22 kHz
30 Hz - 19 kHz (±3 dB)
20 Hz - 20 kHz
ATRS: The following performance is obtained with almost all tapes on the market at present.
UD-ER (NOR) 30 Hz - 18 kHz (±3 dB)
40 Hz - 15 kHz (±1.5 dB)
20 Hz - 20 kHz
UD-EX (CrO₂) 30 Hz - 20 kHz (±3 dB)
40 Hz - 15 kHz (±1.5 dB)
20 Hz - 20 kHz
FeCr 30 Hz - 18 kHz (±3 dB)
40 Hz - 15 kHz (±1.5 dB)
20 Hz - 20 kHz
Metal: 30 Hz - 20 kHz (±3 dB)
40 Hz - 15 kHz (±1.5 dB)
20 Hz - 20 kHz

S/N (Signal to Noise Ratio):
Dolby NR OFF: 60 dB (Weighted A, Reference 3% THD Metal tape)
Dolby NR ON: 69 dB (Weighted A, Reference 3% THD Metal tape)
Wow and Flutter: 0.023% (WRMS)
Input Sensitivity and Impedance:
Microphone: 0.5 mV, 300 ohms-5 kohms
Line in: 85 mV, 100 kohms or more
DIN (Record/Playback): 0.5 mV, 4.7 kohms
Output Level: 775 mV
Output Load Impedance:
Line out: 50 kohms or more
DIN (Record/Playback): 50 kohms or more
470 kohms or more*
Headphone: 8 ohms-2 kohms
Distortion:
Crosstalk: 1.0% (1 kHz 0 dB-3 dB)
Between tracks: 60 dB (at 1 kHz)
Between channels: 30 dB (at 1 kHz)
Power Supply:
AC 120V, 60 Hz (U, C)
AC 100–110V/115–127V/
200–220V/230–250V,
50/60 Hz (W)
AC 220V, 50 Hz (FS)
AC 240V, 50 Hz (BS, AU)
Power Consumption: 37W
Dimensions: 165(H) x 435(W) x
256(D) mm
Weight: 8.7 kg
Motor: Uni-Torque motor x 1
DC motor x 1
Heads: New close gap Metal R & P heads (ferrite)
Double-gap Metal erase head (Permalloy)
ATRS specifications:
Microcomputer used: 4-bit
1-chip microcomputer
Bias variation steps: 32
Sensitivity & Equalization adjustment steps: 32each
(variable by 0.25 dB per step)
Batteries used (for memory protection): “IEC SR44”
x 2

* According to DIN 45 500
## TECHNICAL INFORMATION

### 1. Operation in various modes

<table>
<thead>
<tr>
<th>Mode of deck</th>
<th>Operation details of unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Power OFF</td>
<td>• Only the RAM of the microprocessor is kept live by the battery to hold data.</td>
</tr>
</tbody>
</table>
| 2 Just after power is turned ON    | • Back-up mode is released and also the tape selector control data, immediately before power was turned OFF, is fed to latch circuit of IC501. The data output terminal operates as a key input terminal after that and the unit enters the watch-and-wait mode for key operation.  
  • When data is not present in the memory selected, the memory indicator flashes. |
| 3 Power ON other than testing      | • Key input "Watch-and-wait" mode.                                                      |
|                                    | • Back-up battery voltage compared. Comparison and detection are always done when power is switched ON. |
|                                    | • Record using test memory data or tape select memory data.                             |
| 4 Set for testing                  | • Test mode is set when the Test button is pressed and when the mode control IC output (PLAY, REC, PAUSE) of the mechanism is set to "001". |
| 5 During testing                   | • Testing is performed according to the test items shown in Table 1.                    |
| 6 Immediately after testing is complete | • Data obtained is fed to latch circuit of IC501 after testing is complete.              |
2. Back-up mode

When the power switch is set to OFF or when the power fails instantaneously, the microprocessor and memory (RAM) which stores the internal test data and memory data are kept active by the external power supply (silver oxide battery) while other circuits stop operation. In this mode, the power consumption is reduced and data is stored in the RAM when the power voltage (Vcc) drops to 2.0V. This function is called the back-up mode.

**Operation of the back-up mode**

Terminal 19 (CE) of IC601 shown in Fig. 1 is the back-up input terminal; when this terminal is set to Lo level, the unit enters the back-up mode. Terminal 15 (RESET) is the reset input terminal; when the power is turned on, the back-up mode is released, this terminal changes to Lo from Hi and the START program instruction is given.

The time sequence, shown in Fig. 2, is required for setting and releasing the back-up mode.

That is:

To release the back-up mode, CE terminal should be set to Hi more than 100μs after the power switch was turned ON and the power voltage (Vcc) has been stabilized at +5V. RESET terminal should be set to Lo after a further 100μs or more has elapsed.

To enter the back-up mode, CE terminal should be set to Lo immediately after the power switch is turned OFF and the power voltage should be kept at +4.5V for more than 100 μs. The lowest power voltage which can hold data is 2V. The following circuit operation is performed in this time sequence.

When the power switch is set to ON, +9V power supply is applied to the power terminal 27 of the microprocessor via the +6V constant voltage circuit which is composed of Q211, ZD207. Simultaneously, Q212 is activated and Q213 is turned OFF, so CE terminal is set to Lo, and RESET terminal set to Hi.

Approx. 100 ms after the rise of the +6V power supply, negative voltage rectified through D232 rises to the voltage to cancel normal bias of Q212, so Q212 is OFF and CE terminal becomes Hi. After a further 100 ms, the charging voltage of C233 rises to the operation point of Q213, so Q213 is activated and RESET terminal is set to Lo.

When the power switch is set to OFF, the +6V and -5V power supply voltages drop. However, the charge of C241 cannot flow in reverse because of D238, so it is held. Accordingly, when the +6V power supply voltage drops to 5.4V, Q214 is normally biased, so Q214 is activated, the charge of C241 is applied to the base of Q211 via Q214, D237 and R256, Q211 is activated and CE terminal is set to Lo potential. Simultaneously, the charge of C233 is rapidly discharged via D233 and Q212 to make the reset operation certain in case there is an instantaneous power failure and restoration or power switch OFF/ON operation.
3. Back-up voltage detection/alarm circuit

The back-up voltage detection/alarm circuit shown in Fig. 3 is provided to indicate the residual charge of the back-up battery and presence/absence of memory data. IC504—② and peripheral circuits compose the blocking oscillation circuit; when the power switch is turned ON, assuming the +5V constant voltage power supply is used as reference voltage (V1), it compares this voltage with the back-up battery voltage (V2), and when V2 is smaller than V1, this circuit starts oscillations. Battery alarm indicator LED501 starts flashing due to these oscillations. IC504—① and peripheral circuits detect the back-up battery voltage as well.

When the back-up voltage drops to T1 (power voltage which can hold data) shown in Fig. 4, immediately after this circuit clears data in the memory (RAM) inside the microprocessor, the power switch is turned ON, making 4 tape select indicators flash to warn that no data is held and it inhibits mechanical operation. Pressing one of the 4 tape select buttons releases the mechanical operation inhibition mode. This operation stops the flashing of the 4 tape select indicators and the indicator corresponding to the pressed tape select button flashes. At the same time, the tape select memory indicator starts flashing to warn of the absence of data in the memories.
4. ATRS circuit

(1) Outline of ATRS circuit

Fig. 6

Fig. 6 is a block diagram of the ATRS circuit. When testing starts, the microprocessor controls the oscillation operation and the frequency of the test signal oscillation circuit, and in addition supplies control data to the REC low/medium/high frequency EQ circuit and REC bias circuit to the record and play back calibration signals. PLAY gain at that time is detected and calculated to obtain optimum REC equalization & bias control data so that frequency response is flat and distortion in the range of 40 Hz - 15 kHz is minimized for almost any cassette tape at present on sale. At the same time, it controls the test indicator to give information of the test conditions. Furthermore, it detects the number of revolutions of the reel disc and controls the mechanism control logic to rewind the tape to the test start point after the testing is complete. Table 1 shows the test procedure, items and details. Fig. 7 shows L channel REC/PLAY output and testing time during testing with cassette tape HITACHI UD-ER.
<table>
<thead>
<tr>
<th>Sequence</th>
<th>Test items</th>
<th>Test signal oscillation frequency</th>
<th>Details of test</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>REC sensitivity</td>
<td>1 kHz</td>
<td>Roughly adjusts REC sensitivity with control data from low/medium/high frequency REC equalizer &amp; REC bias circuit set to “10000”.</td>
</tr>
<tr>
<td>2</td>
<td>Error detection</td>
<td>1 kHz</td>
<td>Checks whether or not the test tape is faulty, or the leader tape section is recorded and played back. When the test tape is faulty or leader tape is recorded/played back, it stops testing, instructs the mechanism to stop and starts the test memory indicator flashing.</td>
</tr>
<tr>
<td>3</td>
<td>UP direction REC bias test</td>
<td>1 kHz</td>
<td>Records and plays back 1 kHz reference signal and obtains the bias value when the PLAY level is max. with the REC bias current varied from min. to max. Then, in the same way, obtains the bias value when PLAY level is a max. with REC bias current varied from Max. to Min. Obtains average of these 2 bias values and outputs data with bias value 1 step more than this value.</td>
</tr>
<tr>
<td>4</td>
<td>DOWN direction REC bias test</td>
<td>1 kHz</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Low freq. EQ test</td>
<td>1 kHz</td>
<td>Determines control data so that REC/PLAY output at 7 kHz and 15 kHz is within ±0.5 dB of REC/PLAY output at 1 kHz through testing 3 times.</td>
</tr>
<tr>
<td>6</td>
<td>Medium freq. EQ test</td>
<td>7 kHz</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>High freq. EQ test</td>
<td>15 kHz</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Low freq. EQ test</td>
<td>1 kHz</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Medium freq. EQ test</td>
<td>7 kHz</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>High freq. EQ test</td>
<td>15 kHz</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Low freq. EQ test</td>
<td>1 kHz</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Medium freq. EQ test</td>
<td>7 kHz</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>High freq. EQ test</td>
<td>15 kHz</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Error detection</td>
<td>1 kHz</td>
<td>Checks whether or not the tested section is the leader tape section. When it is the leader tape section, it stops testing, clears obtained data, instructs mechanism to stop operation and starts the test memory indicator flashing.</td>
</tr>
<tr>
<td>15</td>
<td>Rewind up to test start point</td>
<td>1 kHz</td>
<td>REW signal &amp; STOP signal are given to mechanism to rewind the tape to the start point.</td>
</tr>
</tbody>
</table>

Table 1
(2) Circuit operation

1) Test signal oscillation circuit

![Circuit Diagram]

Fig. 8

The test signals required for test items shown in Table 1 are obtained from the test signal oscillation circuits in IC502, shown in Fig. 8. The principles for the oscillation are the same as D-5500, so they are omitted. Table 2 shows the oscillation operation of the microprocessor and the oscillation select control output data.

<table>
<thead>
<tr>
<th>Oscillation condition</th>
<th>Oscillation operation control (D13)</th>
<th>Oscillation frequency control</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>D12</td>
<td>D11</td>
</tr>
<tr>
<td>Oscillation stops</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>During oscillation operation</td>
<td>1 kHz</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>7 kHz</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>15 kHz</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 2
A single IC is used for the discrete low/medium/high frequency EQ circuits, latch circuits, MPX circuits, the U/A converters for REC bias control/PLAY gain detection and Amp, for playback output amplification used in the D-5500. Fig. 9 shows the internal structure of the IC. The output signal of the test oscillation circuit is input to terminal 29, and audio signal of line-in, mic, etc. to terminal 26.

These input signals select the test signal during testing and the audio signal in other modes, by means of the test mode signal supplied to terminal 27 from the microprocessor, to supply them to the next EQ amp.

EQ Amp 1 — EQ Amp 4 are gain varying amps, which determine the bandwidth of low/medium/high frequency band by capacitors, resistors and coils connected to terminals 18, 17, 20 - 23, and control the gain with 5-bit data at terminals 5-9.

The 5-bit data input to terminals 5-9 for gain control is D/A converted through D/A converters iD/A 1 — D/A 3) to control the gain. D/A converter D/A 4 is used for the signal which controls the external REC bias circuit and PLAY gain detection circuit; the REC bias circuit is controlled by IC501L, and the PLAY gain detection circuit by IC501R.

Data applied to the D/A converters for the total of 8 circuits (both L/R channels) requires a total of 40 bits; to minimize the number of input/output terminals, data is given by selecting the circuit by a time sharing system, and when data is not changed it is held by the latch circuit. Selection of the latch circuit to which the 5-bit data is applied is determined by the 2-bit EQ selection signal (terminals 10, 11) which selects 1 latch circuit among the 4 in 1 chip, and by 1-bit channel selection signal (terminal 12) which selects IC501L or IC501R and concurrently provides data entry timing.

Table 3 shows the latch circuits and selected data corresponding to each of the 4 latch circuits.
Terminal 2 of IC501 shown in Figs. 9 & 10 sets the output level change during single step variation of overall variation amount (32 steps) of the control data. To reduce selection noise generated when data is changed due to changing the tape selector, etc., Q602 is cut off by the selection noise preventive control output (Terminal 3) of the microprocessor to minimize the voltage drop at both ends of R902 and the output level change in a single step until the tape position control data is transferred. After the data transfer is complete, the voltage is gradually increased to the set voltage for a single step variation by means of the charging time constant of C606. The control data is output from the microprocessor in the cases mentioned below. In other modes, the control data is held by the latch circuit inside IC501. The data output terminals of the microprocessor operates as key input terminals during data holding.

1) Immediately after the power switch is set to ON
2) Immediately after the tape selector is changed
3) During testing
4) Immediately after testing is complete

Fig. 11 shows the data transfer timing chart for the total of 8 circuits of both L & R channels.

<table>
<thead>
<tr>
<th>Stored memory</th>
<th>Control data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Channel selection</td>
</tr>
<tr>
<td>L ch (IC501L)</td>
<td>D2 D3 R20 R21</td>
</tr>
<tr>
<td>Low freq. EQ AMP</td>
<td>0→1 0 0 0</td>
</tr>
<tr>
<td>Medium freq. EQ AMP</td>
<td>0→1 0 1 0</td>
</tr>
<tr>
<td>High freq. EQ AMP</td>
<td>0→1 0 0 1</td>
</tr>
<tr>
<td>REC bias D/A</td>
<td>0→1 0 1 1</td>
</tr>
<tr>
<td>R ch (IC501R)</td>
<td></td>
</tr>
<tr>
<td>Low freq. EQ AMP</td>
<td>0 0→1 0 0</td>
</tr>
<tr>
<td>Medium freq. EQ AMP</td>
<td>0 0→1 1 0</td>
</tr>
<tr>
<td>High freq. EQ AMP</td>
<td>0 0→1 0 1</td>
</tr>
<tr>
<td>PLAY gain detection D/A</td>
<td>0 0→1 1 1</td>
</tr>
</tbody>
</table>

Table 3

0→1: When data changes from 0 to 1, data is entered to the memory. When it is “0”, data is in the latch mode.
3) REC bias/erasure circuit

The erasure head is driven by the erasure oscillator circuit composed of Q707, Q708; power to the oscillation circuit is increased to obtain the high demagnetization effect needed with Metal Tape. That is, Q711 shown in Fig. 12 is activated to minimize the voltage drop of R726.

Erase oscillator output is supplied to the base of Q705 and Q706 of the REC bias circuit to perform oscillations while synchronizing the erasure oscillator circuit and REC bias circuit. As a result, beats between the 2 oscillation circuits do not occur and variations in the output of the REC bias circuit do not affect the erase oscillator circuit, so completely stable erasure can be obtained.

The REC bias control D/A output obtained from terminal 14 of IC501L as REC bias control is supplied to terminal 5 of IC802. Output from terminal 7 of IC802 is divided by thermistor (TH701), R716, R717, and the voltage drop across R717 is applied to the negative feedback input terminal of IC802. Thermistor (TH701) increases REC bias as the temperature drops, to compensate for the temperature characteristics of the head. VBE of Q709 is controlled by the output of IC802 to vary the power voltage of the REC bias circuit. Q702 is activated and negative feedback to IC802 is minimized to increase the REC bias during the use of Metal Tape.

The erase circuit continues operation and only the REC bias circuit stops operation to reduce noise during the REC/PAUSE mode. That is, REC bias control signal muting transistor (Q712) is controlled by the collector potential of the head plate control transistor (Q204). In the PAUSE mode, the head plate solenoid does not operate, so Q204 is OFF. Q712 is activated by the collector potential HI of Q204 at that time, so REC bias control output of IC802 drops to around 0V, Q709 is cut off and only the REC bias circuit stops operation.
4) Key input circuit/key input inhibit circuit

Fig. 13

Key input
The relationship between the 7 types of key input and 4-bit key input from the microprocessor are shown in Table 4. They are obtained by synchronizing the L/R selection signal output from D8 of the microprocessor. That is, L/R selection signal is inverted every 20 ms, and Q903, shown in Fig. 13, is activated at Hi potential, so the key input shown in Table 4 (Item (1) — (4) ) is detected. At Lo potential, Q904 is activated, so the key input shown in Table 4 (Item (5) — (7) ) is detected. Q903 and Q904 operate in opposite ways so key input does not overlap. When there are 2 or more key inputs to the 4-bit input, operations are ignored.

Key input inhibit
Key input terminals R10 — R13 are concurrently used as REC equalizer/bias & A/D control data output terminals; key input during output of data is inhibited. Output terminal ② of IC601 shown in Fig. 13 is set to Lo potential during output of data from terminals R10 - R13, Q903 and Q904 are cut off and key input is inhibited.

<table>
<thead>
<tr>
<th>Item</th>
<th>Type of key input</th>
<th>L/R output</th>
<th>Key input code</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>D8 R13 R12 R11 R10</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Normal</td>
<td>1 0 1 1 1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>CrO₂</td>
<td>1 1 0 1 1</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Metal</td>
<td>1 1 1 0 1</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>FeCr</td>
<td>1 1 1 1 0</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Test</td>
<td>0 0 1 1 1</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Test Memory</td>
<td>0 1 1 0 1</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Memory</td>
<td>0 1 1 1 0</td>
<td></td>
</tr>
</tbody>
</table>

Table 4
5) Test signal indicator

Progression for testing Items (1) - (13) shown in Table 1 is indicated externally by the test progress indicators (1 kHz, 7 kHz, 15 kHz). A 3-bit signal is obtained from the microprocessor, as shown in Table 5, to control the test progress indicators, shown in Fig. 14.

<table>
<thead>
<tr>
<th>Test indicators</th>
<th>Control data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>D13</td>
</tr>
<tr>
<td>1 kHz</td>
<td>1</td>
</tr>
<tr>
<td>7 kHz</td>
<td>1</td>
</tr>
<tr>
<td>15 kHz</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 5

When the control data shown in Table 5 is set to "1", the indicator (LED) corresponding to that output lights up; one indicator on the higher frequency side lights first and the lighting of other indicator on lower frequency side is prevented.

That is, the 1 kHz indicator lights when D13 output signal of the microprocessor is "1" but D13 output data must also be "1" to light the 7 kHz or 15 kHz indicators, so, to prevent the 1 kHz indicator from lighting at that time, "1" output is set to "0" via D507, Q504 to light the 7 kHz indicator and via D506, Q503 to light the 15 kHz indicator to cut Q505 off.

By the same operational principle, the 7 kHz indicator control signal D11 is also prevented from lighting during the lighting of the 15 kHz indicator.
6) Mechanism input/output control during testing

![Circuit Diagram](image)

**Fig. 15**

1) Mechanism mode input
The mechanism condition is detected by the mode output (PLAY, REC, PAUSE) of IC201 shown in Fig. 15 when testing starts; when the circuit is in the REC mode or tape running mode, the test mode is set. Mechanism mode input at this time results in the data shown below:

- R00 (PLAY): 0
- R01 (REC): 0
- R02 (PAUSE): 1

2) Detection of reel disc rotation pulses
Revolutions of the reel disc generate pulses via the reel disc rotation detection reed relay and the time constant circuit; they are supplied to terminal 30 of the microprocessor to perform interruption processing during testing and are counted.

By this, the tape distance during testing is detected; this is assumed to be the distance to be rewound to the test start position after testing is complete.

3) Test stop input
This input stops the test mode when any of the REW button, STOP button and PAUSE button is pressed during testing.

<table>
<thead>
<tr>
<th>Mode of Deck</th>
<th>IC201 mode output</th>
</tr>
</thead>
<tbody>
<tr>
<td>During testing</td>
<td>PLAY</td>
</tr>
<tr>
<td>When STOP button is pressed during testing</td>
<td>0→1</td>
</tr>
<tr>
<td>When REW button is pressed during testing</td>
<td>0→1</td>
</tr>
<tr>
<td>When PAUSE button is pressed during testing</td>
<td>0→1</td>
</tr>
</tbody>
</table>

Table 6

* Values inverted by Q210 before being supplied to the differential circuit are shown.

The REW, STOP, or PAUSE mode output of IC201 shown in Fig. 15 is supplied to the differential circuit composed of R228 — R230, C226 — C228, and the output from each differential circuit is set to AND-logic using D225 — D227, and supplied to INT1 of the microprocessor.

Table 6 shows the output variation when the STOP, REW or PAUSE button is pressed during testing.
A positive pulse is generated at the terminal the output of which changes from 0 to 1 and this pulse stops the test mode.

**Mechanism control output**

This applies REV & STOP instruction at the test start position when testing is complete. Q401 is activated only when test mode output terminal 1 of the microprocessor is set to Hi potential, that is only during testing, and grounds the emitters of Q208 and Q209 to prevent mis-operation when static electricity pulses enter Q208, Q209.

7) **Key indicators**

Fig. 16 shows the key indicator circuit corresponding to key input. FeCr, Metal and CrO₂ outputs of terminals 66–68 of IC601 become REC, PLAY equalizer and REC bias circuit selection signals as well as indicator control signals.

The TEST mode output signal is set to Hi potential until the head plate solenoid stops after testing starts. Q105 detects head plate solenoid control output and controls test mode output.
8) PLAY gain detection circuit

The play gain detection circuit supplies control data to the REC equalization and REC bias circuits to record the test signal, it detects PLAY output at this time and converts the analog signal to a digital signal. Fig. 17 shows the PLAY gain detection circuit. The circuit is composed of an amplifier circuit, sample hold circuit, L/R input selection circuit and comparison circuit (A/D conversion), and the following control is performed by the microprocessor.

1) Muting monitor signal
Activates Q104 during testing and mutes monitor signal.

2) Resetting sample hold circuit
Charge held by C807 is discharged by activating Q801 before testing items (1) — (14) shown in Table 1. R806 prevents oscillations during resetting.

3) L/R input selection
Input selection of the comparison circuit is performed to detect PLAY output of both L/R channels by one comparison circuit. That is, the L/R selection signal of IC601 is inverted by inverter Q802, controls the L channel PLAY output muting transistor (Q803L). R channel PLAY output muting transistor (Q803R) is directly controlled by the L/R selection signal.

Accordingly, Q803L and Q803R operate oppositely; when the L/R selection signal is “1”, PLAY output of L channel is selected, and when the L/R selection signal is “0”, PLAY output of R channel is selected. Assuming the charge held in C807L is V1L, L channel comparison input voltage (V0L) is obtained from the following formula.

\[
V_{0L} = V_{1L} \times \frac{R_{810R}}{R_{810R} + R_{810L} + R_{810R}}
\]

R channel comparison input voltage is obtained in the same way.

4) D/A control
5-bit data is supplied to IC501R to form a programmable comparison voltage to PLAY input signal of comparator (IC801), and D/A converted DC output is supplied to the comparator through terminal 34. The comparison output between PLAY input and D/A is read every time the 5-bit data increases by 1 step. Data is added until both input voltages shown in Fig. 18 coincide, the comparison output is set to Lo potential and then reaches Hi potential again.

---

Fig. 17

---

Fig. 18
5. Three-phase uni-torque motor

(1) Outline of construction

Fig. 19 shows the outline of the three-phase uni-torque motor. The rotor is composed of a main body to give it a moment of inertia, and a disc magnet split into 8-poles. The stator is composed of a yoke to complete the magnetic circuit, a stator coil, a base board to hold the stator coil, a support and a top plate. In addition, there is a shaft to connect the rotor and stator with bearing, thrust and speed detection FG gears. The stator coil is composed of ball-shaped coils connected in series, with three-phase-Y-connection. Hall elements are used for position detection of the rotor; 3 Hall elements are incorporated in the coil.

(2) Motor drive circuit

The drive system connects one end of the three-phase stator coil in star connection and the other end with three-phase-Y connection which drives using the transistor shown in Fig. 20 to apply power in both directions from a single power supply.

With this system, driving using a sine wave is best from the point of view of torque ripple and external disturbances (noise or vibration) during the selection of current. The unevenness of sensitivity of the rotor position detection Hall element and the effect of offset of the output voltage are large, however, so the sine wave position detection signal obtained from the position detection Hall element is sliced through both upper and lower reference potentials as shown in Figs. 22, 23 to produce a trapezoid wave which is supplied to the stator coil. Since the bias current of the Hall element is supplied by the 2 upper/lower reference currents, the position signal proportional to the difference between the two reference potentials can be obtained. As a result, the waveform does not change when the potential difference changes and the amplitude of the trapezoid wave applied to the stator coil changes. Selection of drive current is not done so rapidly, so external disturbances such as noise or vibration, etc. are small. The three-phase drive voltage is sliced at the common reference potential, the amplitude is uniform and it is not affected by unevenness in the sensitivity of the Hall element.
The lower reference potential is fixed using zener diode and the upper side reference potential is varied by means of the control signal. The neutral potential of the trapezoid wave varies depending on the variation of the control signal but the potential of the output terminal of the Hall element always changes to this neutral potential, so the selection position of the current does not change.

Fig. 23 Position detection of phase and drive circuit

(3) Speed control

![Diagram of speed control system]

Fig. 24

1) Speed detection

![Diagram of speed detection system]

A detection system which uses the coil to detect variations of magnetic resistance due to combinations of gears is employed for speed detection. That is, magnetic force generated by the magnet shown in Fig. 25 flows to gear (B) fixed to the rotor, gear (A) fixed to top plate and yoke in sequence. Magnetic resistance is generated at that time due to the gap between gear (A) and gear (B).

When gear (A) and gear (B) are positioned at point (A) shown in Fig. 26, the gap is minimized, so magnetic resistance decreases. When they are positioned at (B), the gap is larger and magnetic resistance increases. Since the number of teeth of the gear is set at 68, magnetism varies 68 time per 1 turn of the rotor; this variation of magnetism is 412 Hz at the rated speed which is detected by the coil.

![Diagram of gear positions]

Fig. 26
2) f-v conversion

FG signal detected by the coil is supplied to Servo control IC HA-11713, amplified and rectified, and produces the next triangular wave generating pulse through the pulse generator. Discharge pulse width is determined by the resistor connected to terminal 1 and the capacitor connected to terminal 3.
After resetting the next triangular wave generation circuit by means of the discharge pulse, the capacitor connected to terminal 1 is charged until the next discharge pulse is input. So, charging/discharging is repeated every time a discharge pulse is input and the triangular wave voltage is generated.
This triangular wave voltage is held by the next sample hold circuit and the held voltage is output through terminal 13.

3) Comparison

The f-v converted signal obtained from terminal 13 of IC1 passes through the low-pass filter composed of R5 and C6 shown in Fig. 28, and then compared after phase & temperature compensation by the next differential amp.
The reference voltage is stabilized by Zener diode (ZD1), while diode (D7) is inserted for temperature compensation.
For phase compensation, the Amp. (IC2)'s frequency response is determined by R11, R12, C8, the cut-off frequency of the closed loop is set to approx. 25 Hz and loop gain is made larger while minimizing the gain at the speed detection frequency, 412 Hz, using delay compensation.
The upper side sliced section of the position signal, detected and amplified by the Hall elements shown in Fig. 22, is determined by this output (VSH). The reference voltage is further divided by R8 and R9, and voltage drop (Vsl) across R9 is assumed to be the sliced section on the lower side.
<table>
<thead>
<tr>
<th>Terminal No.</th>
<th>Terminal symbol</th>
<th>Terminal name</th>
<th>Terminal functions</th>
<th>During testing</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 42</td>
<td>D3  D2</td>
<td>Channel selection and data writing signal output</td>
<td>Output only when Tape selector changed-over.</td>
<td>Writing positions to IC501 for 8 types of data (Low/medium/high frequency EQ data x 2 ch, Bias data, A/D data) output from terminals 26 - 29, 40 are determined by R20, R21, and writing to IC501 of both L/R CHs is selected by D3 (R CH), D2 (L CH). Writing is performed when D3 or D2 changes from 0 to 1.</td>
</tr>
<tr>
<td>32 33</td>
<td>R20  R21</td>
<td>Equalizer selection signal output</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>D4</td>
<td>Key input inhibition output</td>
<td>Inhibits change of Test, Memory, Tape selector, etc. during Test operation (0: INHIBIT)</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>D5</td>
<td>Data change noise preventive output</td>
<td>Prevents noise generated in latch of IC501 when data is changed during testing or when tape selector is changed. (1: Change-over noise prevention)</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>D6</td>
<td>STOP signal output</td>
<td>Outputs STOP signal to Logic IC to inhibit mechanism operation when the tape is rewound, to Test Start position or when power is switched ON with back-up battery voltage less than specified value (R03 is 0 potential). (1: STOP)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type of output data</th>
<th>Control data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Channel select data</td>
</tr>
<tr>
<td></td>
<td>D2</td>
</tr>
<tr>
<td>L CH</td>
<td>Low freq. EQ</td>
</tr>
<tr>
<td></td>
<td>Medium freq. EQ</td>
</tr>
<tr>
<td></td>
<td>High freq. EQ</td>
</tr>
<tr>
<td></td>
<td>Bias</td>
</tr>
<tr>
<td>R CH</td>
<td>Low freq. EQ</td>
</tr>
<tr>
<td></td>
<td>Medium freq. EQ</td>
</tr>
<tr>
<td></td>
<td>High freq. EQ</td>
</tr>
<tr>
<td></td>
<td>A/D</td>
</tr>
</tbody>
</table>

0→1 : Writing is performed at the point where 0 changes to 1.
<table>
<thead>
<tr>
<th>Terminal No.</th>
<th>Terminal name</th>
<th>Terminal functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>D7</td>
<td>REW signal output</td>
</tr>
<tr>
<td>6</td>
<td>D8</td>
<td>L/R select output</td>
</tr>
<tr>
<td>7</td>
<td>D9</td>
<td>A/D reset output</td>
</tr>
<tr>
<td>8</td>
<td>D10</td>
<td>Test oscillation control output</td>
</tr>
<tr>
<td>9</td>
<td>D11</td>
<td>Test oscillation frequency output</td>
</tr>
<tr>
<td>10</td>
<td>D12</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>D13</td>
<td>Test mode output</td>
</tr>
<tr>
<td>12</td>
<td>D14</td>
<td>Test memory indicator output</td>
</tr>
<tr>
<td>13</td>
<td>D15</td>
<td>Memory indicator output</td>
</tr>
<tr>
<td>14</td>
<td>DNC</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>RESET</td>
<td></td>
</tr>
</tbody>
</table>

**Operation during testing:**
- Outputs REW signal to Logic IC to rewind tape to Test Start position when EC, Bias test is complete. (1: REW)
- Selects input of L CH and R CH during PLAY gain detection.
- Controls operation of test oscillation circuit.
- Varies test oscillation frequency according to tested circuit.

<table>
<thead>
<tr>
<th>Oscillation frequency</th>
<th>Control data</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 kHz</td>
<td>0</td>
</tr>
<tr>
<td>7 kHz</td>
<td>1</td>
</tr>
<tr>
<td>15 kHz</td>
<td>1</td>
</tr>
</tbody>
</table>

**Operation other than testing:**
- Outputs test mode signal from test start until rewind completed.
- Outputs 1 after test starts.
- Inputs whether the test data is present or not in the memory of the tape selector.
- Outputs 0 when Test memory button is pressed and Test data corresponding to the type of tape selected at that time is present.
- Output showing start of program when power (15V) is applied to microprocessor or backup of the battery is released.
- (1: Reset operation)
<table>
<thead>
<tr>
<th>Terminal No.</th>
<th>Terminal symbol</th>
<th>Terminal name</th>
<th>Terminal functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td></td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>OSC 1</td>
<td>Clock oscillation frequency setting input</td>
<td>Clock oscillation frequency built into the microprocessor is determined by resistor (91kΩ) connected between these terminals. Oscillation frequency: 400 kHz</td>
</tr>
<tr>
<td>18</td>
<td>OSC 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>CE</td>
<td>Memory back-up mode input</td>
<td>Input which signals back-up mode, hold memory data or the condition before power is OFF, when the power switch is set to OFF. (0: Back-up mode)</td>
</tr>
<tr>
<td>20</td>
<td>TEST</td>
<td></td>
<td>Always connected to Vcc.</td>
</tr>
<tr>
<td>21</td>
<td>Vcc</td>
<td>Power input</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>R00</td>
<td>PLAY mode input</td>
<td>PLAY: R00 = 0</td>
</tr>
<tr>
<td>23</td>
<td>R01</td>
<td>REC mode input</td>
<td>REC: R01 = 0</td>
</tr>
<tr>
<td>24</td>
<td>R02</td>
<td>PAUSE mode input</td>
<td>PAUSE: R02 = 0</td>
</tr>
<tr>
<td>25</td>
<td>R03</td>
<td>Memory back-up voltage input</td>
<td>Compares the memory back-up battery voltage with the reference voltage when power is set to ON. Inputs 1 when the battery voltage is higher than the reference voltage and inputs 0 when it is lower.</td>
</tr>
<tr>
<td>26</td>
<td>R10</td>
<td>EU, B as data output &amp; key input</td>
<td>8 types of test or memory data are output synchronized with select signals from terminals ①, ②, ③, ③, ③ when the power switch is set to ON or the tape selector is changed. After data output is complete, they become key input shown in the table below, synchronized with L/R select signal of terminal ⑥.</td>
</tr>
<tr>
<td>27</td>
<td>R11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>R12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>R13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>D0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type of key input</td>
<td>L/R output</td>
<td>Key input code</td>
<td></td>
</tr>
<tr>
<td>------------------</td>
<td>------------</td>
<td>----------------</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Terminal</td>
<td>Terminal</td>
<td>Terminal</td>
</tr>
<tr>
<td>Nor</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>CrO₂</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>FeCr</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Metal</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Test</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Test memory</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Memory</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

30 INT0  Reel disc pulse input  Revolutions of reel disc are detected and input using a reed relay to detect tape running distance from test start position up to completion of test of EQ and Bias.

31 INT1  Test stop input  Operation input which stops test operation when STOP, PAUSE or REW is operated during test operation.

34 R22  Not used

35 R23

36 R30  FeCr output  Output according to type of tape

37 R31  Metal output

38 R32  CrO₂ output

39 R33  Nor. output

41 D1  A/D conversion  0 or 1  Inputs 1 when A/D conversion is complete.
SERVICE POINTS

Cautions on handling
This unit performs back-up using a silver oxide battery to keep RAM of the C-MOS microprocessor live to maintain the test data and the condition just before the power was turned OFF, when the power switch is set to OFF. When the voltage of the back-up battery drops to less than the specified value, the data held in the RAM is lost when the power switch is set to OFF; and when the power switch is set to ON again, the operation of the mechanism is inhibited. The 4 tape indicators flash in this inhibition mode.
Perform the operation shown below when the mechanism operation is inhibited.
1) Select a tape selector
   This releases the inhibition mode of the mechanism. However, no test data is present in the RAM as it is, so perform testing.
2) Replace battery
   Replace battery with the power switch set to ON. When the battery is replaced with the power switch set to OFF, normal operation may not be possible. In this case, remove the battery with the power switch set to OFF then reinsert the battery after setting the power switch to ON.
3) This unit is adjusted so that (01011); data is output to the recording equalizer and bias controller of the ATRS circuit when the "NOR" tape selector button is pressed and optimum recording is possible using HITACHI UD-ER tape.
   This (01011)2 data can easily be set during service checking, so use this data for troubleshooting of overall frequency response, etc. (Refer to Item 8 of adjustment).

Cautions on using MOS IC
1. The MOS ICS are inserted into a black sponge for shipment. This sponge is conductive and is used to prevent destruction by short-circuiting between leads. Do not remove the IC from this sponge during storage. Avoid removing ICs from the sponge and do not place on plastic which is likely to be charged with static electricity or insert it into styrofoam.
2. Be sure to ground the soldering iron or use a low voltage soldering iron for soldering because a high voltage may be applied due to a leakage from the soldering iron.
3. The worker should be grounded during work because the human body, clothes made from synthetic fibres, nylon gloves, etc., may be charged with several thousand volts of static electricity.
4. Be sure to ground measuring instruments such as oscilloscopes, VTVMs, etc. when they are used.

DISASSEMBLY

1. Top Cover
   ![](image1)

2. Front Panel
   ![](image2)
3. Sub Panel

4. Peak Level Meter Cover

5. Peak Level Meter

6. ATRS PC Board

7. Bottom Cover

8. Cassette Chassis

B3 x 4

BT3 x 10

Nylon rivet

Open

BT 3 x 10

BT 3 x 10

Chassis bracket

BT 3 x 10

BT 3 x 10

BT 3 x 10

BT 3 x 10

BT 3 x 10

(from bottom side)
# ADJUSTMENT

* According to DIN 46 500.

<table>
<thead>
<tr>
<th>Item</th>
<th>Adjustments</th>
<th>Measuring instrument &amp; connection</th>
<th>Tape used/check tape</th>
<th>Condition of set</th>
<th>Adjusted position</th>
<th>Adjusted value</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Cleaning</td>
<td>Cleaning head, capstan, pressure roller, etc.</td>
<td>RECORD LINE</td>
<td>MAX.</td>
<td>OUTPUT</td>
<td>MAX.</td>
<td>DOLBY NR</td>
</tr>
<tr>
<td>2</td>
<td>Setting of switches &amp; knobs</td>
<td>Set switches &amp; knobs as shown in table below when otherwise not specified.</td>
<td>RECORD, MG</td>
<td>MIN.</td>
<td>MONITOR TAPE</td>
<td>TAPE SELECT</td>
<td>NOR</td>
</tr>
<tr>
<td>3</td>
<td>Tape speed</td>
<td>• Frequency counter</td>
<td>LINE OUT</td>
<td>MT-111 (0,000 Hz)</td>
<td>3150 Hz</td>
<td>21 Hz</td>
<td>150 Hz</td>
</tr>
<tr>
<td>4</td>
<td>RECORD/playback head</td>
<td>• Head adjusting tab</td>
<td>————</td>
<td>————</td>
<td>————</td>
<td>————</td>
<td>————</td>
</tr>
<tr>
<td>5</td>
<td>Source monitor level</td>
<td>• Audio oscillator (400 Hz)</td>
<td>LINE IN</td>
<td>Terminal (6) of MOD21L, R</td>
<td>0.775 V</td>
<td>PLAY</td>
<td>RT21L, R</td>
</tr>
<tr>
<td>6</td>
<td>Digital peak meter</td>
<td>• Audio oscillator (400 Hz)</td>
<td>LINE IN</td>
<td>Terminal (6) of MOD21L, R</td>
<td>0 dB</td>
<td>PLAY</td>
<td>RT101L, R</td>
</tr>
<tr>
<td>7</td>
<td>PLAY gain</td>
<td>• V.T.V.M.</td>
<td>————</td>
<td>Terminal (6) of MOD21L, R</td>
<td>MT-150 (400 Hz)</td>
<td>25 m</td>
<td>PLAY</td>
</tr>
<tr>
<td>8</td>
<td>Setting control data</td>
<td>*This unit can supply &quot;NOR&quot; tape position control data (010111) to the equalizer/bias circuits by the following procedure. Adjust as follows so that frequency response is within the specification while this data is applied:</td>
<td>IC501L (bias control output)</td>
<td>V.T.V.M.</td>
<td>Terminal (6) of IC501L</td>
<td>————</td>
<td>PLAY</td>
</tr>
<tr>
<td>9</td>
<td>Control</td>
<td>• IC501R (A/D control output)</td>
<td>V.T.V.M.</td>
<td>Terminal (6) of IC501R</td>
<td>————</td>
<td>PLAY</td>
<td>RT601R</td>
</tr>
<tr>
<td>10</td>
<td>REC bias adjustment</td>
<td>• Audio oscillator (1.5 kHz/15 kHz)</td>
<td>LINE IN</td>
<td>LINE OUT</td>
<td>HITACHI UD-ERIC-900</td>
<td>REC/PLAY</td>
<td>RT701L, R</td>
</tr>
<tr>
<td>11</td>
<td>REC level adjustment</td>
<td>• Audio oscillator (1 kHz)</td>
<td>LINE IN</td>
<td>LINE OUT</td>
<td>HITACHI UD-ERIC-900</td>
<td>REC/PLAY</td>
<td>RT602L, R</td>
</tr>
<tr>
<td>12</td>
<td>TEST oscillation output</td>
<td>• Synchroscope</td>
<td>BETWEEN side of C606 &amp; ground</td>
<td>————</td>
<td>————</td>
<td>REC/PLAY</td>
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Volume PC Board

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**RESISTORS**

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Note:
Components marked without numbers in this drawing are not specified as replacement parts.
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**FOR CASSETTE DECK ASSEMBLY (A)**

**FOR CASSETTE DECK ASSEMBLY (B)**

**MISCELLANEOUS**
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**Type of head**

- **P** Pan head screw
- **BT** Binding head tapping screw
- **F** Flat countersunk head screw
- **BL** Bolt
- **B** Binding head screw
- **W** Washer
- **T** Round head tapping screw
- **E** "E" ring

When ordering hardware excluding stated on these lists, be sure to make your orders with type and size.
HITACHI SALES CORPORATION OF AMERICA
Eastern Regional Office
1200 Wall Street West, Lyndhurst, New Jersey 07071
Tel. 201-935-8980

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Tel. (0043222) 439367/8

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Tel. 95-8722

HITACHI Ltd. TOKYO JAPAN
Head Office: 5-1, 1-chome, Marunouchi, Chiyoda-ku, Tokyo
Tel. Tokyo (212) 1111 (80 lines)

Cable Address: "HITACHI" TOKYO
Codes: All Codes Used

Printed in Japan (K)
TROUBLESHOOTING

This troubleshooting manual describes examples of faults and methods of investigating causes. Use this manual together with the previously issued Service Manual No. 1302.

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SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

STEREO CASSETTE TAPE DECK

January 1981  TOKAI WORKS
1. FAULTY RISING OF BIAS

When the sound gradually rises during the STOP → REC mode in the condition in which the signal is input; the bias oscillator increases/decreases the bias current by controlling the power voltage of the oscillator using IC802 and Q709.

Check variation when the STOP mode is changed to the REC mode.

- Is the voltage rise on the C702 side fast?
  - Yes: Is the rise of IC802 pin 7 fast?
    - Yes: Is the rise of IC802 pin 6 smooth?
      - Yes: IC501L faulty
    - No: R702, C701 faulty
  - No: R725, C702 faulty

- Q712, R730, R269, R268, R267, C242 faulty.
- C242 side and R265 GND side short-circuited with IC802 pin 6.

2. HEAD DOES NOT LIFT UP

Check the power voltage (≈ 5V) of IC201 first, when does not FF, REW etc.

- Is PLAY indicator lit?
  - Yes: Is it set to Hi during PLAY with IC201 pin 3 open?
    - Yes: Does the Head plate lift up with the Q204 collector grounded?
      - Yes: Q204, D213 faulty. Q204 base circuit faulty.
      - No: Does the Head plate lift up with the Q204 collector grounded?
        - No: D212 malfunction. Set so it is not possible to pull them mechanically.
    - No: IC201 faulty
  - No: Does IC201 pin 3 change to 0V from 2.2V when the PLAY button is pressed?
    - Yes: IC201 pin 3 set to 0V?
      - Yes: P1 connector, GND lifted. Mechanism SW PCB faulty
      - No: IC201 pin 3 and GND are short-circuited
    - No: IC201 faulty

3. TEST LAMP DOES NOT GO OFF

When the TEST lamp (1 kHz) of ATRS does not go off after testing is complete; Approx. 5V positive pulse is generated by D225 ~ 7, C226 ~ 8, R228 ~ 32 and Q210, and input to Microprocessor pin 3, when testing is completed the lamp goes off; in the 3 cases in which the unit comes out of the PLAY mode, when the unit enters the PAUSE mode during testing, or when the unit comes out of the REW mode during rewinding after testing.
4. REC/PLAY L, R DO NOT MATCH

Is the tape monitor level of source +2 dB when the adjusting data is set, and 1 kHz 23 VU is recorded and played back using a HITACHI ER/UD tape?

Yes

Test ATRS

No

Adjust RT602 L, R

When RT602 L, R cannot be adjusted:
1. Setting bias current inadequate
2. IC501 L, R faulty
3. RT601 L, R adjusted poorly

When RT801 L, R cannot be adjusted:
1. IC501 L, R faulty
2. A/D circuit faulty

- A/D circuit faulty
Pull out P23 L, R and input 0 dBm 20 dB (1 kHz) from the external oscillator. Or set the standard data and input 0 22 dB (1 kHz and record/play back the signal. Set RT801 L, R to the neutral point. Check the level of each section at that time.
- The output of IC501 L, R pin 4 is approx. 6 dBm. (The OP amp. of IC501 may oscillate at that time depending on the VTM during measurement. Insert a 10 kΩ resistor in series with the input and perform measurement.)
- DC voltage at side of C807 is approx. 1V (Measure using a digital voltmeter IC801, D801 L, R faulty.

- L/R switching circuit using Q802, Q803 L, R faulty.
Is the voltage changed by L/R switching at IC802 pin 2?

Yes

Q802, Q803 L, R, R209 open, etc.

No

Does IC802 pin 1 change from Lo to Hi during testing?

Yes

Does microprocessor Pin 4 change from 0V to 5V during testing?

Yes

Microprocessor IC501 faulty

No

D802, 803 faulty

No

IC802, R904R, R905R faulty, is IC501 pin 1 adjusted properly?
5. REC MUTING IS NOT DONE

Does it mute with B — E of Q902 short-circuited?

<table>
<thead>
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</thead>
<tbody>
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</tbody>
</table>

Is the REC MUTE indicator lit?

<table>
<thead>
<tr>
<th>Is the contact of R908 and R906 set to GND level with MUTE switch ON?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yes</td>
</tr>
<tr>
<td>No</td>
</tr>
</tbody>
</table>

12V power supply faulty

<table>
<thead>
<tr>
<th>12V power supply faulty</th>
</tr>
</thead>
<tbody>
<tr>
<td>R929 faulty</td>
</tr>
<tr>
<td>Q902 faulty</td>
</tr>
</tbody>
</table>

Key switch connector faulty.

<table>
<thead>
<tr>
<th>Key switch connector faulty</th>
</tr>
</thead>
<tbody>
<tr>
<td>R906 faulty</td>
</tr>
</tbody>
</table>

Yes

<table>
<thead>
<tr>
<th>Key switch connector faulty</th>
</tr>
</thead>
<tbody>
<tr>
<td>R906 faulty</td>
</tr>
</tbody>
</table>

No

<table>
<thead>
<tr>
<th>Key switch connector faulty</th>
</tr>
</thead>
<tbody>
<tr>
<td>D901, RL901 faulty</td>
</tr>
</tbody>
</table>

6. HIGH FREQUENCY DETERIORATED

Cause:

1. When the high frequency is deteriorated due to a faulty head, or faulty adjustment in another section of the circuit during the setting of adjustment data, and it is corrected by bias control, the bias value may become unbalanced between L and R.

The optimum bias value is detected on the R CH side during ATRS test, and L CH follows it, so the bias value may become inadequate.

2. When the high frequency is deteriorated during source monitoring: MPX filter faulty, soldertouch, etc.

3. When the AF oscillator for ATRS testing is not adjusted properly.

4. Head magnetized

7. DISTORTION GREAT

Cause:

1. When the bias current is inadequate due to (1) in item 6 above.

2. Muting circuit faulty. Q107 L, R, Q104 L, R, etc. (Try to set C — E open.)

3. Head faulty.

8. ATRS DOES NOT OPERATE

(When TEST error occurs)

Cause:

1. When RT801 L, R is set to minimum.

2. When RT602 L, R is poorly adjusted.


4. Microprocessor faulty (especially pin 4).

5. Level deteriorated due to dirt — etc. on the head.

6. When the testing oscillator is not operating. (Is approx 4 dBm output to C506 ⊗ side?)
9. ATRS DOES NOT MEMORIZE DATA  
(All the tape selector LEDs flash)

- Does BATT indicator flash?
  - Yes
  - No

- Is BATT indicator lit when a 3V power supply is connected in place of batteries?
  - Yes
  - No

  - Replace batteries
    - (Insert batteries with power ON)
  - Is battery power consumption during power OFF approx. 2.5 µA?
    - Yes
    - No

- D508 open
  - Yes
  - No

10. ATRS SYSTEM

(1) 15 kHz TEST indicator is kept lit.
The oscillation of the microprocessor and the oscillation frequency switching control output data are given in the table below.

<table>
<thead>
<tr>
<th>Oscillation</th>
<th>Oscillation control (D13)</th>
<th>Oscillation frequency control D12</th>
<th>Oscillation frequency control D11</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillation stop</td>
<td>0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>During oscillation operation</td>
<td>1 kHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>7 kHz</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>15 kHz</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

The oscillation frequency during testing is controlled by the output as shown in the table above. The ATRS test indicator uses the signal and lights up.

- Is IC601 pin 16 set to Hi?
  - Yes
  - No

- Is IC601 pin 16 kept at 5V while it is lifted?
  - Yes
  - No

- Microprocessor faulty
  - Yes
  - No

- Q503 faulty
  - Yes
  - No

D505, 506 faulty.
P43: (3) short circuited with GND.
(2) Battery indicator does not light.

- **D501, 504 faulty**
  - No
  - Is voltage of IC504 pin 5 smaller than that of IC504 pin 6
    - Yes → IC504 faulty
    - No
      - Is D503 anode set to approx. 3V?
        - Yes → Batteries inserted in reverse. P39, 40 in reverse.
        - No → 2V or more
          - Yes → Is IC504 pin 7 set to 0 voltage?
            - Yes → Is IC504 pin 6 set to approx. 6V?
              - Yes → LED faulty. Both terminals of LED short-circuited
              - No → Batteries exhausted. replace them (insert them with power ON) or when 0V, one battery is in reverse.
            - No → Is power consumption during power OFF smaller than 3 μA?
              - Yes → C510 short-circuited. D904 short-circuited
              - No → OK
      - No → -3V
        - Yes → 0 → 2V
          - Is power consumption during power OFF smaller than 3 μA?
            - Yes → C510 short-circuited. D904 short-circuited
            - No → OK

(3) Indicator of FeCr (or Tape select LED) does not light.

- Do Nor. CrO₂, Metal tape LEDs light?
  - Yes → Is IC601 pin 5 set to Hi when FeCr tape is used?
    - Yes → Is IC901 pin 6 set to Lo?
      - No → 5V power supply faulty.
    - No → Does IC601 pin 6 //[underline] // at 20 msec intervals?
      - Yes → Is IC601 pin 2 set to Hi?
        - Yes → D908 open. Microprocessor faulty.
        - No → Microprocessor faulty
      - No → Does TEST memory indicator light?
        - Yes → FeCr SW faulty. Panel PCB faulty.
        - No → IC901 faulty

**Q903 open. Q904 short-circuited. O802 open.**
11. RECORDING SYSTEM
(1) Enters the ERASE or RECORD mode during PLAY.

<table>
<thead>
<tr>
<th>Is REC indicator lit?</th>
<th>No</th>
<th>Is recording possible with Q703 C — E short-circuited?</th>
<th>Yes</th>
<th>Is Q704 collector set to approx. 26V?</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Yes</td>
<td></td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Q710 faulty</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>No</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yes</td>
<td></td>
<td></td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Yes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yes</td>
<td></td>
<td>IC201 pin 7 short-circuited to GND. IC201 faulty.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

12. REC/PLAY FREQUENCY RESPONSE OF LOW FREQUENCY TOO BOOSTED
Cause:
(2) ATRS test performed with tape position confused.
(3) C602 L, R faulty.

13. IMMEDIATELY STOPS WITH STOP → PLAY OPERATION
(Especially reduced voltage)
Cause:
(1) Regulation of the 5V power supply is not satisfactory for some reason, and the reset circuit operates with little load fluctuation.
(2) C211 → Capacity small, D206 — 209 disconnected (connect diodes in parallel to check it).
(3) D237, 238 short-circuited, Q214 faulty.
This cassette deck is the same as the model D-3300M [silver] except that it has the black appearance.

The table below shows the different points from D-3300M [silver], so use together with the D-3300M [silver] Service Manual (No. 1302) issued previously.

**REPLACEMENT PARTS LIST**

<table>
<thead>
<tr>
<th>SYMBOL-NO.</th>
<th>P-NO.</th>
<th>DESCRIPTION</th>
<th>P-NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>86</td>
<td>6630998</td>
<td>CASSETTE METAL ASSEMBLY</td>
<td>6630995</td>
<td>CASSETTE METAL ASSEMBLY</td>
</tr>
<tr>
<td>95</td>
<td>6203912</td>
<td>METER FILTER ASSEMBLY</td>
<td>6203911</td>
<td>METER FILTER ASSEMBLY</td>
</tr>
<tr>
<td></td>
<td>8699410</td>
<td>BT BIND HEAD SCREW-3MMD x 10MM (BLACK) [FOR CASSETTE METAL MOUNTING]</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8737408</td>
<td>FLAT SCREW-3MMD x 8MM (BLACK) [FOR 11P MOULD SOCKET MOUNTING]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>101</td>
<td>6671774</td>
<td>FRONT PANEL</td>
<td>6671772</td>
<td>FRONT PANEL</td>
</tr>
<tr>
<td>102</td>
<td>6223324</td>
<td>SUB PANEL ASSEMBLY</td>
<td>6223322</td>
<td>SUB PANEL ASSEMBLY</td>
</tr>
<tr>
<td>103</td>
<td>6757832</td>
<td>FUNCTION METAL ASSEMBLY</td>
<td>6757831</td>
<td>FUNCTION METAL ASSEMBLY</td>
</tr>
<tr>
<td>105</td>
<td>6257723</td>
<td>FUNCTION BUTTON ASSEMBLY</td>
<td>6257721</td>
<td>FUNCTION BUTTON ASSEMBLY</td>
</tr>
<tr>
<td>106</td>
<td>6257724</td>
<td>FUNCTION BUTTON ASSEMBLY (STOP)</td>
<td>6257722</td>
<td>FUNCTION BUTTON ASSEMBLY (STOP)</td>
</tr>
<tr>
<td>107</td>
<td>6533372</td>
<td>EARTH SPRING</td>
<td>6533371</td>
<td>EARTH SPRING</td>
</tr>
<tr>
<td>108</td>
<td>6052753</td>
<td>PUSH BUTTON ASSEMBLY</td>
<td>6052751</td>
<td>PUSH BUTTON ASSEMBLY</td>
</tr>
<tr>
<td>109</td>
<td>6052722</td>
<td>EJECT BUTTON ASSEMBLY</td>
<td>6052721</td>
<td>EJECT BUTTON ASSEMBLY</td>
</tr>
<tr>
<td>111</td>
<td>6052742</td>
<td>RESET BUTTON</td>
<td>6052741</td>
<td>RESET BUTTON</td>
</tr>
<tr>
<td>115</td>
<td>6092512</td>
<td>CASSETTE DOOR ASSEMBLY</td>
<td>6092511</td>
<td>CASSETTE DOOR ASSEMBLY</td>
</tr>
<tr>
<td>116</td>
<td>6052762</td>
<td>PUSH BUTTON ASSEMBLY (POWER)</td>
<td>6052761</td>
<td>PUSH BUTTON ASSEMBLY (POWER)</td>
</tr>
<tr>
<td>117</td>
<td>6296704</td>
<td>KNOB (TIMER)</td>
<td>6296701</td>
<td>KNOB (TIMER)</td>
</tr>
<tr>
<td>118</td>
<td>6052732</td>
<td>BUTTON ASSEMBLY (MEMORY, PEAK HOLD)</td>
<td>6052731</td>
<td>BUTTON ASSEMBLY (MEMORY, PEAK HOLD)</td>
</tr>
<tr>
<td>119</td>
<td>6669783</td>
<td>FUNCTION KNOB</td>
<td>6669781</td>
<td>FUNCTION KNOB</td>
</tr>
<tr>
<td>120</td>
<td>6669773</td>
<td>KNOB (OUTPUT)</td>
<td>6669771</td>
<td>KNOB (OUTPUT)</td>
</tr>
<tr>
<td>121</td>
<td>6287594</td>
<td>KNOB ASSEMBLY (RECORD L)</td>
<td>6287592</td>
<td>KNOB ASSEMBLY (RECORD L)</td>
</tr>
<tr>
<td>122</td>
<td>6289184</td>
<td>KNOB ASSEMBLY (RECORD R)</td>
<td>6289182</td>
<td>KNOB ASSEMBLY (RECORD R)</td>
</tr>
<tr>
<td>123</td>
<td>6043374</td>
<td>UPPER COVER (U)</td>
<td>6149428</td>
<td>UPPER COVER (U)</td>
</tr>
<tr>
<td>124</td>
<td>6043374</td>
<td>UPPER COVER (BS)</td>
<td>6149427</td>
<td>UPPER COVER (BS)</td>
</tr>
<tr>
<td>128</td>
<td>6796123</td>
<td>FELT LEG</td>
<td>6796121</td>
<td>FELT LEG</td>
</tr>
<tr>
<td>132</td>
<td>8671420</td>
<td>BT BIND SCREW-3MMD x 20MM</td>
<td>7781146</td>
<td>BT SCREW-3MMD x 20MM</td>
</tr>
<tr>
<td>133</td>
<td>8699610</td>
<td>BT BIND SCREW-4MMD x 10MM (BLACK)</td>
<td>7781731</td>
<td>BT BIND SCREW-4MMD x 10MM (BLACK)</td>
</tr>
</tbody>
</table>

**SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT**

**STEREO CASSETTE TAPE DECK**

April 1981

TOKAI WORKS